IN THE CLAIMS

1. (Original) A semiconductor device comprising:

a plurality of gate lines composed of line shapes to function as gate electrodes in a plurality of transistors and separated from a semiconductor layer by a gate insulating layer, each gate line having an upper metal silicide layer;

a plurality of source/drain regions formed on said semiconductor layer between said gate lines solely by carrying out impurity implantation processes.

2. (Original) The semiconductor device according to claim 1, wherein said semiconductor layer is formed of a silicon substrate.

3. (Original) The semiconductor device according to claim 1, wherein said impurity implantation processes are carried out by a dose of impurity below 1.0×10^{15} ions/ cm^2.

4. (Original) The semiconductor device according to claim 1, wherein said metal of said metal silicide layer is one selected from the group consisting of Co and Ti.

5. (Withdrawn) A method of manufacturing a semiconductor device comprising the steps of:

forming a gate insulating layer on a semiconductor substrate;

forming a silicon gate layer on said gate insulating layer;

forming gate lines by patterning said silicon gate layer;

performing an impurity implantation by using said gate lines as a mask;

forming an interlayer insulating layer over said substrate over which said impurity implantation is carried out;

exposing said silicon gate layer of said gate lines by planarizing said interlayer insulating layer; and

forming a metal silicide layer on an exposed surface of said silicon gate layer.

6. (Withdrawn) The method of manufacturing a semiconductor device according to claim 5,

further including the steps of forming openings to expose a given region of said substrate by partially etching said interlayer insulating layer after said step of forming said interlayer insulating layer, and filling said openings by depositing a silicon layer; and

wherein said step of exposing said silicon gate layer of said gate lines includes planarizing said silicon layer.

7. (Withdrawn) The method of manufacturing a semiconductor device according to claim 5, wherein said step of forming said metal silicide layer comprises:

depositing a metal layer by a sputtering process;

annealing said metal layer; and

removing non-reacted residual metal by an etching process.

8. (Original) A flash memory device comprising:

an active region comprising a plurality of line shaped sub-regions, each being formed parallel to each other by means of an isolation layer on a substrate in a cell area;

at least one common source line formed of wall shaped silicon material to be in contact with and cross said active region, having an upper metal silicide layer;

a plurality of gate lines formed parallel to said common source line, arranged in order from both sides of said common source line to be symmetric with respect to said common source line and separated from said active region by said gate insulating layer, each having an upper metal silicide layer;

a plurality of source/drain regions formed in said active region between said gate lines by carrying out impurity implantation;

an interlayer insulating layer formed to cover said gate lines and said common source line;

a plurality of bit lines formed parallel to said active region and connected with at least one of both sides of said gate lines positioned in both ends of said active region through contacts passing through said interlayer insulating layer; and

at least a portion of said gate lines having a layered structure comprising a floating gate of a silicon layer, a separating dielectric layer, and a control gate having a silicon layer and a silicide layer, on each of junction regions on which said gate lines and said active regions cross each other.

9. (Original) The flash memory device according to claim 8, wherein said metal silicide layer of said common source line is formed of the same material and level as those of said metal silicide layers of said gate lines.

10. (Original) The flash memory device according to claim 8,

wherein a half of said gate lines arranged symmetrically with respect to said common source line is composed of a ground select gate line, a plurality of word lines and a string select gate line arranged in order from one of both sides of said common source line; and

wherein on a portion of said junction regions which said word lines among said gate lines are crossed with said active region, a double-layered gate structure in which a floating gate is separated from a control gate by a dielectric layer is formed.

11. (Original) The flash memory device according to claim 8,

wherein said source/drain regions are composed of regions doped by a dose of impurity below 1.0×10^{15} ions/ cm^2.

12. (Original) The flash memory device according to claim 8, wherein each of said contacts is composed of:

a silicon pad having a metal silicide layer formed at the same level as that of said metal silicide layers of said gate lines and said common source line; and

an upper portion composed of the same material as that of said bit lines.

13. (Original) The flash memory device according to claim 12, wherein said bit lines are composed of the same metal material as that for forming said metal silicide layers.

14. (Original) The flash memory device according to claim 8, wherein said gate lines have insulating spacers formed on both side walls thereof, and each of said source/drain regions between said gate lines have a dual doped structure.

15. (Withdrawn) A method of forming a cell area of a flash memory device comprising the steps of:

forming an active region having a plurality of line shaped sub-regions on a semiconductor substrate, each being defined parallel to each other by an isolation layer;

forming a gate insulating layer and a silicon floating gate layer in said active region;

forming a floating gate intermediate pattern by patterning said floating gate layer;

forming a dielectric layer over the whole surface of said substrate over which said floating gate intermediate pattern is formed;

forming a silicon control gate layer over said substrate over which said dielectric layer is formed;

forming a plurality of gate lines in a direction vertical to a direction forming said active region by etching partially said silicon control gate layer, said dielectric layer, and said floating gate intermediate pattern;

doping said active region between said gate lines by using a dose of impurity below 1.0×10^{15} ions/ cm^2;

forming a lower interlayer insulating layer over the whole surface of said substrate over which said doping is carried out;

forming a groove exposing a common source region in said active region by etching partially said lower interlayer insulating layer;

depositing a silicon layer to fill said groove;

forming a wall shaped silicon common source line with exposing upper portions of said gate lines by planarizing said silicon layer and said lower interlayer insulating layer; and

forming a metal silicide layer on exposed upper surfaces of said gate lines and said silicon common source line.

16. (Withdrawn) The method of forming a cell area of a flash memory device according to claim 15, further including the step of forming an etch stop layer over the whole surface of said substrate between said step of doping and said step of forming said lower interlayer insulating layer.

17. (Withdrawn) The method of forming a cell area of a flash memory device according to claim 15,

wherein said step of forming said groove includes forming contact holes in bit line contact regions; and

further including the steps of:

forming an upper interlayer insulating layer after said step of forming said metal silicide layer;

forming contact holes in said bit line regions by etching partially said upper interlayer insulating layer;

depositing a wiring metal layer for bit lines and bit line contacts; and

forming bit lines by patterning said wiring metal layer.